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PO Attainment

Faculty Name: Sweta Agarwal **Class-Sem:** B.Tech. EE V **Academic Year:** 2022-23

Course Name: Computer Architecture **Course Code:** BEE-502 **Program Name:** B.Tech. EE

CO-PO MAPPING:

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	
CO1	2	1			3	1				
CO2	2	1		2				3		
CO3			3		2	1	2			
CO4			1		2			2	3	
CO5	1		2		2					
CO6		2		3			1	2		

CO ATTAINMENT:

Sweta Agarwal	Att. Level
CO1	2.70
CO2	2.70
CO3	2.57
CO4	2.60
CO5	2.60
CO6	2.57

PO ATTAINMENT :

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	
Overall PO Attainment	2.7	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	

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CO Attainment

Faculty Name: Sweta Agarwal **Class/Sem:** B.Tech. EE V **Academic Year:** 2022-23

Course Name: Computer Architecture **Course Code:** BEE-502 **Program Name:** B.Tech. EE

S. No.	University Reg. No.	Student Name	First Unit Test	Second Unit Test	First Class Test	Second Class Test	Best One From Unit Test	Best One Form Class Test	Internal Marks Scheme: Unit Test(UT)	Internal Marks Scheme: Attendance(AT)	Internal Marks Scheme: Teacher Assessment(TA)	Total Internal Marks	End Sem Exam Marks	Total Marks
			Theory (25)	Theory (25)	Theory (10)	Theory (10)	Theory (25)	Theory (10)	10	10	5	Theory (25)	Theory (75)	Theory (100)
1	BEE2020001	Karan Singh	20	16	8	6	20	8	8	8	4	20	22	42
2	LBEE2021007	Faizan Khan	20	16	4	3	20	4	8	8	2	18	12	30
3	LBEE2021006	Mradul Singh	10	8	4	3	10	4	4	4	2	10	23	33
4	LBEE2021002	Shashank	20	16	8	6	20	8	8	8	4	20	21	41
5	LBEE2021004	Himanshu Sharma	25	20	8	6	25	8	10	10	4	24	40	64
6														
7														
8														
9														
10														
		Students appeared for the examination	5	5	5	5	5	5	5	5	5	5	5	5
		Target / satisfactory mark set as benchmark	10	10	4	4	10	4	4	4	2	10	30	40
		Students scored above the target set	5	4	5	3	5	5	5	5	5	5	1	3
		% Students scored above the target set	100%	80%	100%	60%	100%	100%	100%	100%	100%	100%	20%	60%
		Attainment Level	3	3	3	2	3	3	3	3	3	3	1	2

													Overall
CO1	3		3		3	3	3	3	3	3	1	2	2.70
CO2	3		3		3	3	3	3	3	3	1	2	2.70
CO3	3				3		3	3		3	1	2	2.57
CO4		3		2	3	3	3	3	3	3	1	2	2.60
CO5		3		2	3	3	3	3	3	3	1	2	2.60
CO6		3			3		3	3		3	1	2	2.57

Rubric:

% Students	Level
<50%	1
50-75%	2
>75%	3

Overall attainment	2.62

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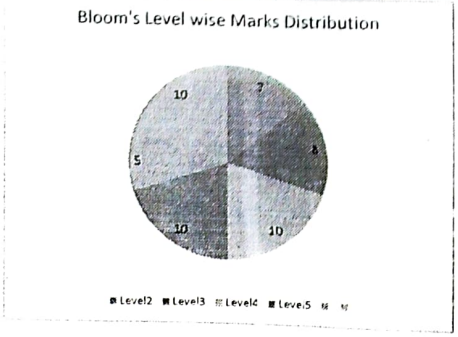
ODD Semester Examination 2022-23
Computer Architecture (BEE-504)
B.Tech. EE- V sem
Maximum Marks :50 ; Duration: 3 Hours

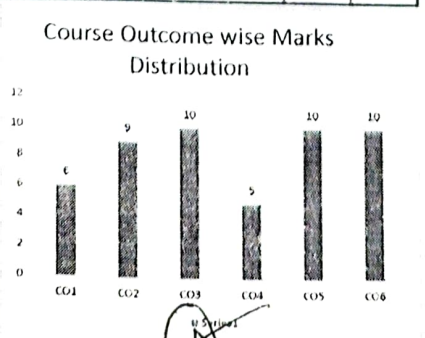
Q.No	Questions	Marks (70)	CO	BL
	Explain the following:			
1-I	(a) What is RISC and CISC?	01	CO1	L2
1-II	(b) What is micro programming?	01	CO2	L1
1-III	(c) What is the role of cache memory?	01	CO2	L2
1-IV	(d) what are the various types of data types ?	01	CO2	L1
1-V	(e) what are bus systems?	01	CO2	L1
	Explain the following:			
2-I	(a) what is PROM and EEROM?	01	CO1	L1
2-II	(b) what are special function registers?	01	CO1	L1
2-III	(c) what is DMA?	01	CO1	L1
2-IV	(d) How many data bus present in the 8086 microprocessor?	01	CO1	L2
2-V	(e) what is segmentation?	01	CO1	L1
3-I	((A) Explain the various cache mapping techniques in detail OR (B) What is the location of cache memory in memory system? Explain with the help of block diagram	5	CO2	L2
3-II	(A) what is interrupts? Explain the hardware interrupts of 8086 microprocessor in detail. OR (B) What is flag register? Explain the flag register of 8086 microprocessor in detail.	5	CO3	L3
4-I	(A) Explain the various secondary memories present in the computer systems.. OR (B) explain the various arithmetic instructions used in the 8086 microprocessor	5	CO3	L5
4-II	(A) Describe the architecture and function of a general computer system. OR (B) What do you understand by bus systems? Differentiate it with multi –bus organization.	5	CO4	L3
5	WQ 5 (a) Draw the Pin diagram of 8086 Microprocessor. And explain it . OR (b) how many address buss are present in the 8086 microprocessor? Explain the architecture of 8086 microprocessor .	10	CO5	L4
6	(a) what is pipelining? Explain the steps to design of basic pipelining OR (b) What are the addressing modes? Explain addressing modes of 8086 in detail.	10	CO6	L6

BL – Bloom's Taxonomy Levels
(1- Remembering, 2- Understanding, 3 – Applying, 4 – Analysing, 5 – Evaluating, 6 - Creating)
CO – Course Outcomes PO – Program Outcomes; PI Code – Performance Indicator Code

Level	Marks
Level1	7
Level2	8
Level3	10
Level4	10
Level5	5
Level6	10
Total	**50**

CO	Marks
CO1	6
CO2	9
CO3	10
CO4	5
CO5	10
CO6	10
Total	**50**





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NAAC

First Unit Test -2022-23

Computer Architecture (BEE-504)

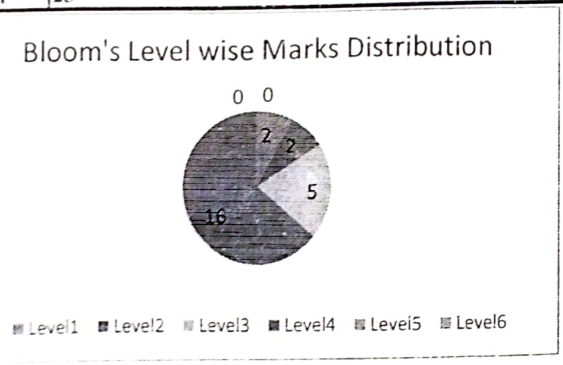
B.Tech, EE- V sem

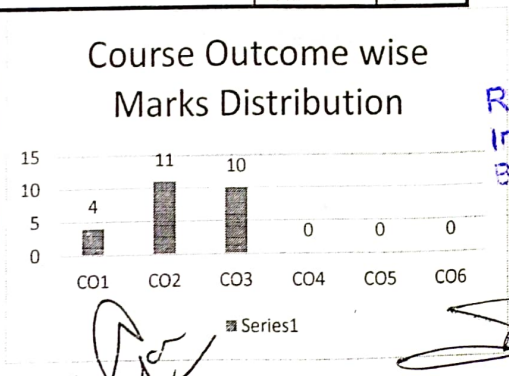
Maximum Marks : 30; Duration: 90 Minutes

Q.No	Questions	Marks (30)	CO	BL
	Attempt All questions.			
1-I	write an example of floating point representation	01	CO1	L1
1-II	write an dexample of fixed point representation	01	CO1	L1
1-III	write the full form of RISC	01	CO1	L2
1-IV	write full form of CISC	01	CO1	L2
2	Discribe control Unit operation OR Differentiate between microprogramming and microinstruction	05	CO2	L3
3-	Describe the architecture and Function of a general Computer. OR Describe various data types.	06	CO2	L4
4	What do you mean by system Buses? Differentiate it with Multi Bus organization. OR Differentiate between CISC and RISC	10	CO3	L4

BL – Bloom's Taxonomy Levels

Level	Marks	CO	Marks
Level1	2	CO1	4
Level2	2	CO2	11
Level3	5	CO3	10
Level4	16	CO4	0
Level5	0	CO5	0
Level6	0	CO6	0
Total	**25**	**Total**	**25**





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Second Unit Test -2022-23

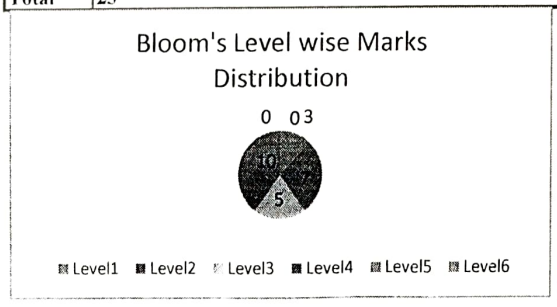
Computer Architecture (BEE-504)

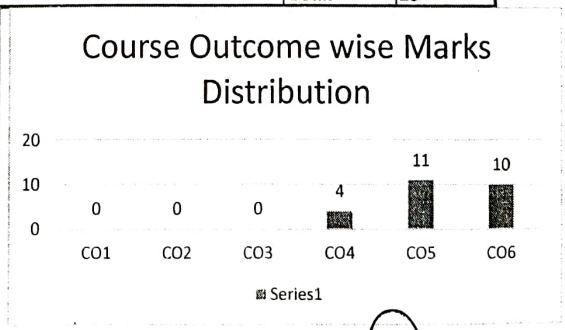
B.Tech. EE- V sem

Maximum Marks :25; Duration: 90 Minutes

Q.No	Questions	Marks (30)	CO	BL
	Explain the following in very short -			
1-I	(a) What is the use of MOV instruction in 8086 microprocessor	01	CO4	L1
1-II	(b) What is pipelining?	01	CO4	L1
1-III	(c) What are PROM and EEROM?	01	CO4	L2
1-IV	(d) How many address bus exist in 8086 microprocessor?	01	CO4	L1
3	Q2. What is the basic concept of designing of pipelining? Explain the execution in pipelining processor. OR Write down the features of 8086 microprocessor. Compare the 8085 and 8086 microprocessor.	05	CO5	L3
4	. Explain the memory structure used in computer architecture. Explain Typical RAM chip using block diagram and function table. OR Draw the memory connection to CPU through data and address bus using 512 bytes of RAM and 512 bytes of RAM.	06	CO5	L2
4-A	Explain the architecture of 8086 microprocessor. Draw the pin diagram of 8086 microprocessor.	10	CO6	L4

BL – Bloom's Taxonomy Levels			
Level	**Marks**	**CO**	**Marks**
Level1	3	CO1	0
Level2	7	CO2	0
Level3	5	CO3	0
Level4	10	CO4	4
Level5	0	CO5	11
Level6	0	CO6	10
Total	**25**	**Total**	**25**





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First Class Test -2022-23

Computer Architecture (BEE-504)

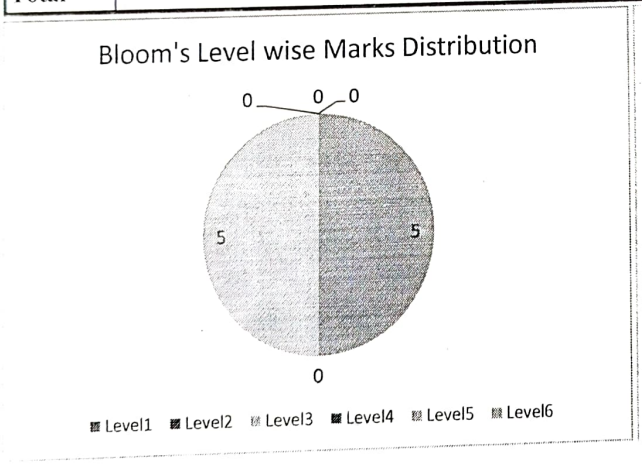
B.Tech. EE- V sem

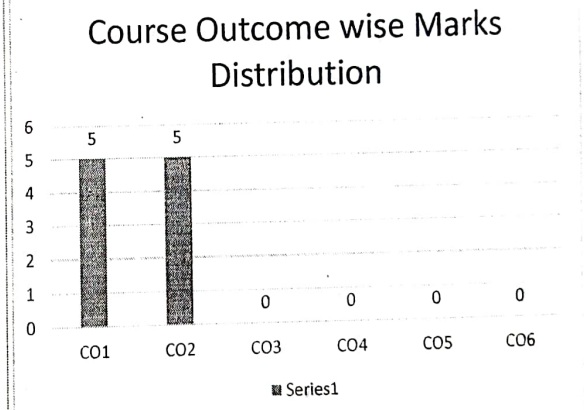
Maximum Marks :10; Duration: 30 Minutes

Q.No	Questions	Marks (10)	CO	BL
1	Differentiate between CISC and RISC	05	CO1	L3
2	Describle the architecture of general Computer.	05	CO2	L1

BL – Bloom's Taxonomy Levels
(1- Remembering, 2- Understanding, 3 – Applying, 4 – Analysing, 5 – Evaluating, 6 - Creating)
CO – Course Outcomes PO – Program Outcomes; PI Code – Performance Indicator Code

Level	Marks	CO	Marks
Level1	5	CO1	5
Level2	0	CO2	5
Level3	5	CO3	0
Level4	0	CO4	0
Level5	0	CO5	0
Level6	0	CO6	0
Total	**10**	**Total**	**10**





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NAAC

Second Class Test -2022-23

Computer Architecture (BEE-504)

B.Tech. EE- V sem

Maximum Marks :10; Duration: 30 Minutes

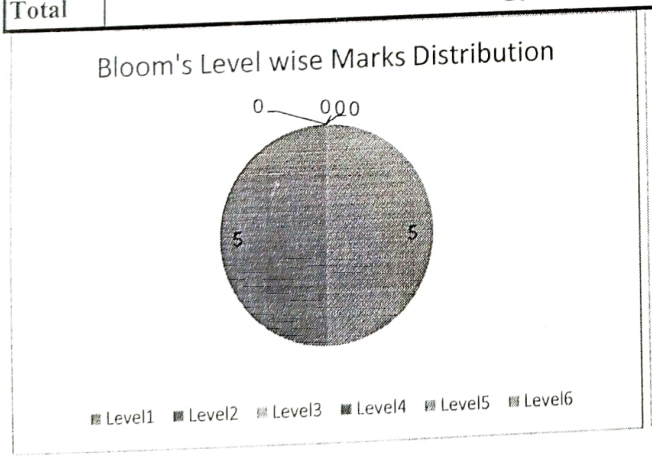
Q.No	Questions	Marks (10)	CO	BL
1	Explain the memory structure used in computer architecture. Explain Typical RAM chip using block diagram and function table.	05	CO4	L2
2	Explain the architecture of 8086 microprocessor. Draw the pin diagram of 8086 microprocessor.	05	CO5	L1

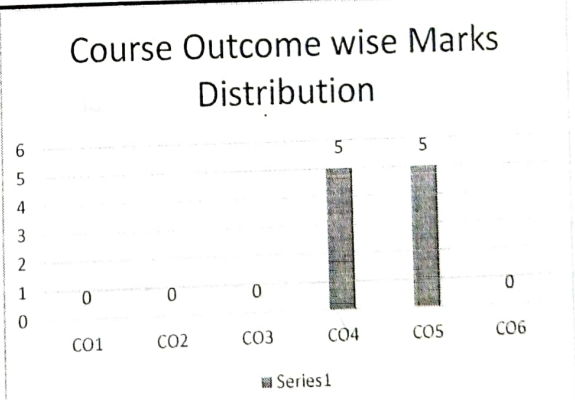
BL – Bloom's Taxonomy Levels

(1- Remembering, 2- Understanding, 3 – Applying, 4 – Analysing, 5 – Evaluating, 6 - Creating)

CO – Course Outcomes PO – Program Outcomes; PI Code – Performance Indicator Code

Level	Marks	CO	Marks
Level1	5	CO1	0
Level2	5	CO2	0
Level3	0	CO3	0
Level4	0	CO4	5
Level5	0	CO5	5
Level6	0	CO6	0
Total	**10**	**Total**	**10**





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Tabulation Sheet

PROGRAM : BACHELOR OF TECHNOLOGY (ELECTRICAL ENGINEERING) (LATERAL ENTRY)
SEMESTER : FIFTH
SESSION : 2022-23
COLLEGE : Faculty of Engineering & Technology

Sl. No.	Enrollment No.	Roll No.	Student ID	Student Name	BEE501					BEE502					BEE503					BEE504					BEE551					BEE552					BEE553					BOE012					BPE501				
					Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR
					50	25	75		3	50	25	75		3	50	25	75		3	50	25	75		3	15	10	25		1	15	10	25		1	15	10	25		1	50	25	75		3	50	25	75		3
					E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS
1	210838	2150305002	LBEE2021004	HIMANSHU SHARMA	42	25	67		3	43	23	66		3	42	23	65		3	40	24	64		3	14	9	23		1	14	9	23		1	14	9	23		1	37	22	59		3	42	23	65		3
2	211194	2150305003	LBEE2021006	MRADUL SINGH	30	10	40		3	27	10	37		3	20	10	30		3	23	10	33		3	12	8	20		1	12	8	20		1	11	7	18	-	1	20	10	30		3	28	10	38		3
3	211790	2150305006	LBEE2021002	SHASHANK	28	16	44		3	28	15	43		3	20	20	40		3	21	20	41		3	13	8	21		1	13	8	21		1	13	8	21		1	22	14	36		3	24	19	43		3
4	210701	2150305001	LBEE2021007	FAIJAN KHAN	24	18	42		3	12	16	28		0	26	20	46		3	12	18	30		3	11	8	19		1	11	8	19		1	12	7	19		1	11	16	27		0	16	15	31		0
5	211372	2150305004	LBEE2021005	PRADEEP KUMAR	AB	0	0		0	AB	0	0		0	AB	0	0		0	AB	0	0		0	AB	0	0		0	AB	0	0		0	AB	0	0		0	AB	0	0		0	AB	0	0		0

Controller of Examination

Registrar

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> CPI of Re-Appear Students are not Calculated.

Legend:-

E - External Marks I - Internal Marks
T - Total Marks
Date : Jan 18, 2023
G - Passed with Grace Marks
CR - Credit

Passing marks - 40% in each course

BEE501 : POWER SYSTEM I (APPARATUS AND MODEL ANA...
BEE502 : CONTROL SYSTEMS
BEE503 : MICROPROCESSORS
BEE504 : COMPUTER ARCHITECTURE
BEE551 : POWER SYSTEMS LABORATORY

INVERTIS UNIVERSITY BAREILLY

Bareilly-Lucknow National Highway, Bareilly - 243123 (UP)

Tabulation Sheet

PROGRAM : BACHELOR OF TECHNOLOGY (ELECTRICAL ENGINEERING) (LATERAL ENTRY)
SEMESTER : FIFTH
SESSION : 2022-23
COLLEGE : Faculty of Engineering & Technology

Sl. No.	Enrollment No.	Roll No.	Student ID	Student Name	BPE501		IIOT15					Grand Total	Credit Secured	SGPA	CPI	Remarks
						CR	Max Marks				CR					
						3	70	30	100		4	625	25			
					G	CS	E	I	T	G	CS					
1	210838	2150305002	LBEE2021004	HIMANSHU SHARMA		3	37	27	64		4	519	25	0.00	59.32	Pass
2	211194	2150305003	LBEE2021006	MRADUL SINGH		3	35	12	47		4	313	25	0.00	34.8	Pass
3	211790	2150305006	LBEE2021002	SHASHANK		3	34	19	53		4	363	25	0.00	40.64	Pass
4	210701	2150305001	LBEE2021007	FAIJAN KHAN		3	33	21	54		4	315	19	0.00	--	PCP- BEE502, BOE012
5	211372	2150305004	LBEE2021005	PRADEEP KUMAR		0	AB	0	0		0		0	0.00	--	Re-Appear- BEE501, BEE502, BEE503, BEE504, BEE551, BEE552, BEE553, BOE012, BPE501, IIOT15

Controller of Examination

Registrar

> CPI of Re-Appear Students are not Calculated.

egend:- - **Passing marks - 40% in each course**

-External Marks I - Internal Marks
- Total Marks

ate : Jan 18, 2023

INVERTIS UNIVERSITY BAREILLY

Bareilly-Lucknow National Highway, Bareilly - 243123 (UP)

Tabulation Sheet

PROGRAM : BACHELOR OF TECHNOLOGY (ELECTRICAL ENGINEERING)
SEMESTER : FIFTH
SESSION : 2022-23
COLLEGE : Faculty of Engineering & Technology

il o.	Enrollment No.	Roll No.	Student ID	Student Name	BEE501					BEE502					BEE503					BEE504					BEE551					BEE552					BEE553					BOE012					BPE501		
					Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks				CR	Max Marks		
					50	25	75		3	50	25	75		3	50	25	75		3	50	25	75		3	15	10	25		1	15	10	25		1	15	10	25		1	50	25	75		3	50	25	7
					E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T	G	CS	E	I	T
1	204564	2010305001	BEE2020001	KARAN SINGH	22	18	40		3	26	16	42		3	20	21	41		3	22	20	42		3	10	7	17		1	10	7	17		1	11	7	18		1	19	16	35		3	12	15	2

Controller of Examination | **Registrar** | **Vice Chancellor**

> CPI of Re-Appear Students are not Calculated.

egend:- **Passing marks - 40% in each course**

-External Marks I - Internal Marks
- Total Marks

ate : Jan 21, 2023

- **Passed** with Grace Marks
R-Credit

BEE501 : POWER SYSTEM I (APPARATUS AND MODELLING)
BEE504 : COMPUTER ARCHITECTURE
BEE502 : CONTROL SYSTEMS
BEE551 : POWER SYSTEMS LABORATORY - I
BEE503 : MICROPROCESSORS
BEE552 : CONTROL SYSTEMS LABORATORY

Tabulation Sheet

PROGRAM : BACHELOR OF TECHNOLOGY (ELECTRICAL ENGINEERING)
SEMESTER : FIFTH
SESSION : 2022-23
COLLEGE : Faculty of Engineering & Technology

Sl. No.	Enrollment No.	Roll No.	Student ID	Student Name	BPE501		HOT15					Grand Total	Credit Secured	SGPA	CPI	Remarks
						CR	Max Marks				CR					
						3	70	30	100		4	625	25			
					G	CS	E	I	T	G	CS					
1	204564	2010305001	BEE2020001	KARAN SINGH		0	31	23	54		4	333	22	0.00	--	PCP- BPE501

Controller of Examination **Registrar** **Vice Chancellor**

> CPI of Re-Appear Students are not Calculated.

Passing marks - 40% in each course

egend:-
-External Marks I - Internal Marks
- Total Marks
ate : Jan 21, 2023
- Passed with Grace Marks
- Credit

BEE501 : POWER SYSTEM I (APPARATUS AND MODELLING)
BEE504 : COMPUTER ARCHITECTURE
BEE502 : CONTROL SYSTEMS
BEE551 : POWER SYSTEMS LABORATORY - I
BEE503 : MICROPROCESSORS
BEE552 : CONTROL SYSTEMS LABORATORY