B.Sc. Forensic Science: Semester-VI FST604: Physics - VI	
Teaching Scheme	**Examination Scheme**
Lectures: 3 hrs/Week	Class Test -12 Marks
Tutorials: 1 hr/Week	Teachers Assessment – 6 Marks
Credits: 4	Attendance – 12 Marks
	End Semester Exam – 70 marks

Course outcomes:

The student at the completion of the course will be able to:

- Study the drift and diffusion of charge carriers in a semiconductor.
- Understand the Two-Port model of a transistor.
- Study the working, properties and uses of FETs.
- Comprehend the design and operations of SCRs and UJTs.
- Understand various number systems and binary codes.
- Familiarize with binary arithmetic.
- Study the working and properties of various logic gates.
- Comprehend the design of combinational and sequential circuits.

Unit I – Semiconductor Junction
• Expressions for Fermi energy, Electron density in conduction band, Hole density in valence band, Drift of charge carriers (mobility & conductivity), Diffusion of charge carries and Life time of charge carries in a semiconductor. Work function in metals and semiconductors. Expressions for Barrier potential, Barrier width and Junction capacitance (diffusion & transition) for depletion layer in a PN junction. Expressions for Current (diode equation) and Dynamic resistance for PN junction.
Unit II – Transistor Modeling
• Transistor as Two-Port Network. Notation for dc & ac components of voltage & current. Quantitative discussion of Z, Y & h parameters and their equivalent two-generator model circuits. h-parameters for CB, CE & CC configurations. Analysis of transistor amplifier using the hybrid equivalent model and estimation of Input Impedance, Output Impedance and Gain (current, voltage & power).
Unit III – Number System
• Number Systems: Binary, Octal, Decimal & Hexadecimal number systems and their inter conversion. • Binary Codes: BCD, Excess-3 (XS3), Parity, Gray, ASCII & EBCDIC Codes and their advantages & disadvantages. Data representation.
Unit IV – Logic Gates
• Truth Table, Symbolic Representation and Properties of OR, AND, NOT, NOR, NAND, EX-OR & EX-NOR Gates. Implementation of OR, AND & NOT gates (realization using diodes & transistor) De Morgan's theorems. NOR & NAND gates as Universal Gates. Application of EX-OR & EXNOR gates as pairty checker. Boolean Algebra. Karnaugh Map.
Unit V – Combinational & Sequential Circuits
• Combinational Circuits: Half Adder, Full Adder, Parallel Adder, Half Substractor, Full Substractor. Data Processing Circuits: Multiplexer, Demultiplexer, Decoders & Encoders. Sequential Circuits: SR, JK & D Flip-Flops, Shift Register (transfer operation of Flip-Flops), and Asynchronous & Synchronous counters.

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