

B.Sc. Forensic Science: Semester-IV	
FST 406: Computer Science- IV	
Teaching Scheme	Examination Scheme
Lectures: 3 hrs/Week	Class Test -12 Marks
Tutorials: 1 hr/Week	Teachers Assessment – 6 Marks
Credits: 4	Attendance – 12 Marks
	End Semester Exam – 70 marks

Course outcomes:

The student will be able to understand

- the basic arithmetic of a Computer System;
- how the data is represented,
- how the various operation are performed on the data, the basic circuits to perform these operations,
- how instructions are formatted and how these instructions are executed to accomplish a particular operation.
- Student can also learn the organization of the peripheral devices, the interface between these devices to the system.
- Student can also understand the architecture of a basic computer, its registers, bus system and the interaction flow among them.

Unit I – Data Representation and basic Computer Arithmetic

- Number systems, complements, fixed and floating point representation, character representation, addition, subtraction, magnitude comparison.
- Logic gates and circuits: logic gates, boolean algebra, combinational circuits, circuit simplification, introduction to flip-flops and sequential circuits, decoders, multiplexers, registers, counters.

Unit II – Basic Computer Organization and Design

- Computer registers, bus system, instruction set, timing and control, instruction cycle, memory reference, input-output and interrupt.
- Central Processing Unit: Register organization, arithmetic and logical micro-operations, stack organization, Hardwired vs. micro programmed control. Pipeline control: Instruction pipelines, pipeline performance, super scalar processing, Pipelining, RISC & CISC

Unit III – Programming the Basic Computer

- Instruction formats, addressing modes, instruction codes, assembly language
- Memory Organization: Memory device characteristics, random access memories, serial access memories, Multilevel memories, address translation, memory allocation, Main features, address mapping, structure versus performance.

Unit IV – Input-output Organization


- Peripheral devices, I/O interface, Modes of data transfer: Programmed, Interrupt Driven and Direct Memory Access.

Unit V – Parallel processing

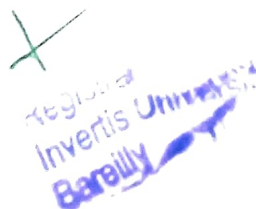
- Processor-level parallelism, multiprocessor architecture


Head

Department of Biotechnology
Invertis University, Bareilly (U.P.)


Dean

Faculty of Science
Invertis University, Bareilly (U.P.)


Regional
Invertis University
Bareilly